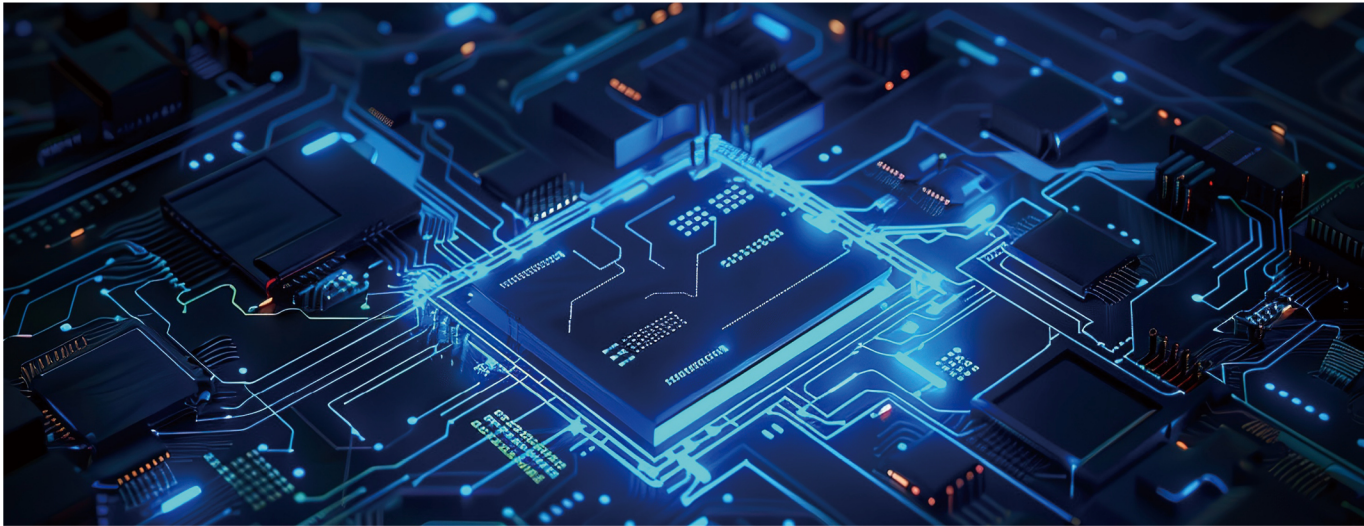


PLD400-BX-48-6

| High Efficiency Non-isolated LLC-DCX Power Card



Description

The PLD400-BX-48-6 is a high efficiency non-isolated LLC-DCX power card with fixed 8:1 ratio, operating from 40-60V DC primary bus voltage to 5-7.5V output voltage and can deliver up to 400W continuous power at typical 54V input voltage.

It is designed to support Artificial Intelligence applications and can also be used for other high-power IBC requirements which have limited board space available.

Applications

- Data center
- DC Power Distribution
- High end computing systems

Features

- Peak efficiency 97.6%
- 27mm*18mm*6.4mm
- High power density IBC up to 2107 W/in³
- Horizontal mounting non- isolated DC/DC converter
- Ratio conversion Ratio conversion 8:1, 400 W continuously, 900 W peak power

Specifications

PLD1000-BX-48-12						
Specifications			Min.	Max.	Units	
Characteristics						
Operating temperature			-20	125	° C	
Storage temperature			-40	125	° C	
Input voltage (Vin) continuous operation			-0.3	60	V	
Input voltage transient			-0.3	68	V	
Cout			0.1	6	mF	
Signal I/O voltage (EN, PG, ALERT, ADDR, SCL, SDA)			-0.3	3.7	V	
Specifications		conditions	Min.	Typ.	Max.	Units
Key features						
Efficiency (η)	Vin=54V, Iout=80A, Tj= 25°C			97.2		%
	Vin=54V, Iout=40A, Tj= 25°C			97.6		%
Pout_TDP thermal design power (TDP)	See Note 1			400		W
Pout_MAX peak power (t ≤ 0.25 s)	See Note 1			900		W
Switching frequency (fs)	0-100 % of Pout_TDP			1250		kHz
Recommended capacitive load			110	470	5000	μF
Input characteristics						
Input voltage range (Vin)			38		60	V
Input idling power	Pout = 0 W				65	W
Input OVP				6.6		V
Internal input capacitance			100	150		μF
Recommended external input capacitance	See Note 2		100	150		μF
Output characteristics						
Output voltage	Pout = 0 W			6.7		v
Output current (Iout)	Vin = 38 - 60 V, PG asserted			60	80	A
Output voltage droop	Iout step from 0 to 80 A			150		mV
Output ripple & noise	20 MHz BW			TBD		mVp-p
Internal output capacitance	Vout = 0V			260		μF
On/off control						
Initialization Time	From Vin > 8.5 V to ready to be enabled			TBD		ms
Turn-off input voltage	Decreasing input voltage			TBD		V
Turn-on input voltage	Increasing input voltage			TBD		V
On Delay Time	From EN asserted to ramp start			TBD		ms
Ramp-up time	From 10% to 90% of Vout, Iout = 0 A			TBD		ms
Start-up time	from Vin connection to 90% of Vout			TBD		ms
Enable start-up time	From EN asserted to 100% of Vout, Iout = 0 A			TBD		ms
Logic high: trigger level	EN pin			0.4		V
Logic low: trigger level	EN pin			2.6		V
Source current	EN pin (Internal pull up)			5		mA
Sink current	EN pin			5		mA

Specifications

PLD1000-BX-48-12					
Specifications	conditions	Min.	Typ.	Max.	Units
Protection features					
Input Under Voltage fault limit (IUVP)	Latch		32		V
Input Over Voltage fault limit (IOVP)	Latch		68		V
Output overvoltage fault limit (OVP)	Latch		7.9		V
Over temperature fault limit (OTP)	Latch		130		°C
Over Current Protection (OCP)	Slow latching	85	90	100	A
Fast latching		150		A	V
Protection response time (IUVP, IOVP, UVP, OVP, OTP, OCP)			TBD		ms
5.0V Vcc Auxiliary power					
Voltage		4.5	5.0	5.5	V
Current				200	mA
Monitoring & Control					
UVLOVI - Under Voltage Lock-Out	Vin rising threshold		8.5		V
	Hysteresis		2.5		V
Power Good Delay Time	From Vout = 100 % to PG asserted		TBD		ms
Power Good Threshold	Low to high transition		100		% V _{out}
	High to low transition, Note 3				
VIL - Logic input low	SCL, SDA			1	V
VIL- Logic input high	SCL, SDA	2.1			V
VOL - Logic output low	SDA, ALERT, PG			0.4	V
IOL - Logic output low sink current	SDA, ALERT, PG		20		mA
ILEAK - Logic leakage current	SDA, SCL, ALERT, PG	-1		1	µA
CI_PIN - Logic input capacitance	SDA, SCL, EN		1.5		pF
Monitoring accuracy					
Input voltage READ_VIN			±1		%
Output voltage READ_OUT			±80		mV
Output current READ_Iout	Vin = 54 V, Iout = 60 A		±5		%
Temperature READ_TEMPERATURE_1			±3		°C

Note 1: Max. output current is rated at 220 A. Max power is < 3000 W and continuous power (thermal design power TDP) is < 1000 W depending on thermal conditions.
Note 2: Typical value (recommended) is 100 µF + 5*10 µF
Note 3: Power Good is deasserted when the output voltage is disabled, regardless of the output voltage level.

Mechanical information

